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An Extensive Study on Different Underlap Architectures for Improved Analog/RF Performance of 32 nm DG-MOSFET

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ABSTRACT

This paper proposed an underlap double-gate MOSFET (U-DG MOSFET) structure with gate stacking. Better sub-threshold slope and RF performance can be obtained from DG MOSFET with symmetrical/asymmetrical drain-source configuration. Simulation shows better results for its upgraded resilient against short channel effects (SCE). The analog and RF performances at 32 nm technology were estimated. Furthermore, the drive capability (on current) of the device, the intrinsic gain (g_mR_o), the transconductance (g_m), and transconductance generation factor (g_m/I_d) were also evaluated. By using non-quasi-static approach, high frequency parameters such as intrinsic (C_{gs} and C_{gd}), parasitic resistance (R_{gs} and R_{gd}), transport delay (τ_m), the unity gain cut-off frequency (f_T), and the maximum frequency of oscillation (f_{max}) were also calculated. A single stage amplifier was then designed to evaluate the performance of the proposed device.

Keyword: Underlap, Asymmetric Structure, Analog Performance, RF Performance, Single Stage Amplifier.

1. INTRODUCTION

In order to achieve low power, small chip area and improved speed; metal-oxide semiconductor field-effect transistor (MOSFET) device dimensions have been aggressively scaled down to nanometer realm. In spite of increase in ON-current, drastic scaling down of the device leads to excessive leakage current. The presence of the leakage current was due to the shrinkage of the channel and associated effect termed as short current effects (SCE) which includes the drain induced barrier lowering (DIBL), threshold voltage roll-off, gate induced drain leakage (GIDL), hot carrier effect, and etc. [1, 2]. The symmetric model of underlap double-gate nMOSFET (U-DG nMOSFET) has emerged as a possible solution for the minimization of the SCE [3-6]. This architecture minimizes the GIDL as well as fringing capacitances, although with reduction in underlap lengths, DIBL become higher. Underlap on the other hand increases channel resistance, which in turn reduces the ON-current. Hence, the underlap length must be optimized for the desired function of the device [7].

With the increasing demands for high-speed devices with low power consumption for various digital and analog applications, more drive current seems to be the primary concern. Therefore, scaling the thickness of gate oxide (t_{ox}) is necessary in order to boost up the gate oxide

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capacitance (C_{ox}). As the result, the ON-current was also enhanced. With the reduction in t_{ox}, gate tunneling process becomes significant, thereby contributing to gate leakage. Therefore, t_{ox} of approximately 1.2 nm is utmost required for proper control over gate tunneling [8]. In order to counter this issue, high-k dielectrics, such as HfO_2 and Al_2O_3 are being used to replace the conventional SiO_2 but keeping the same effective oxide thickness (EOT) [9]. However, the use of high-k dielectrics has its own set of shortcomings, which includes the presence of interface traps and severe scattering. These phenomena cause a reduction in the mobility of the carriers [7,10], which affect the ON-current as well. This can be mitigated by providing a thin layer of SiO_2 between the high-k and the silicon channel because the silicon and oxide junction provides minimal interface traps resulting to reduction of scattering at high extent. This particular arrangement is termed gate stack (GS) [11].

The device with symmetric underlapped (Symmetric-U) structure provides immunity against the SCE, but increased the channel length, which in turn, reduces the ON-current significantly. This is not desirable considering the ever increasing demands for higher ON-current in system-on-chip (SoC) applications. Hence, the concept of asymmetric underlap double-gate (A-U-DG) device comes as a prospective solution. In this paper, we primarily focus on the advantages of removing the underlap on either side of the device. The removal of underlap at the source side gives us the asymmetric drain underlapped (Drain-U) device, whereas removal of drain side underlap gives us the source underlapped (Source-U) device. The performances of both aforementioned devices are compared against the Symmetric-U device under the purview of RF, analog, and circuit analysis. Drain current (I_d), transconductance (g_m), transconductance generation factor (g_m/I_d), DIBL, and intrinsic gain (g_mR_o) are the parameters used to characterize the analog performance. The non-quasi-static (NQS) approach has been used in order to obtain the RF performance of the device including capacitances (C_{gs} and C_{gd}), parasitic resistances (R_{gs} and R_{gd}), the transport delay (τ_m), the unity gain cut-off frequency (f_T), and the maximum frequency of oscillation (f_{max}) [12].

In Section II, the structure of the device along with its specifications, descriptions, and the simulation procedures have been discussed. Section III compares the devices under consideration in terms of analog performances. The RF performances of the structure are examined in Section IV. Section V gives us the circuit level performances of the devices when applied to a single stage amplifier. Lastly, the work is concluded in section VI

2. DEVICE DESCRIPTIONS AND SIMULATIONS

The device parameters and biasing voltages are chosen in accordance with the International Technology Roadmap of Semiconductors (ITRS) roadmap [8]. Table 1 shows the detailed specifications of the proposed device. The following parameters as specified in the Table 1 was chosen: gate length to be 32 nm, EOT is 1.2 nm (consists of a fine layer of SiO_2 and HfO_2), body thickness of 11 nm, n^+ doping to be 10^{20} cm^{-3} and doping in channel region to be 10^{16} cm^{-3}, whereas the optimized underlap length of 21 nm.

Table 1 Parameters used to design the device

Device Parameters	Values
Gate Length	32 nm
Effective Oxide Thickness(EOT) i) Thickness of SiO_2 ii) Thickness of HfO_2	1.2 nm 0.45 nm 4.8 nm
Silicon body thickness	11 nm
Permittivity of Spacer	7.5
Doping in n^+ region	10^{20} cm^{-3}
Doping in Channel region	10^{16} cm^{-3}
Optimized underlap length	21 nm

Figure 1 (a) to (c) shows the different underlap structures. To simulate the devices, density gradient models and drift-diffusion models were employed to amalgamate carrier transport techniques and quantum mechanical properties individually. The Shockley-Read-Hall (SRH) recombination model was incorporated for the recombination process. The Arora mobility model [13] was also utilized due to the dependency of mobility on temperature as well as on doping concentration. Velocity saturation was prepared by deploying the mobility model envisioned by Canali et al. [14]. The effects of high-k mobility degradation and surface roughness scattering are included by utilizing an improved Lombardi model [15], which covers the empirical degradation conditions reporting for surface abruptness obtained from [16] and [17], respectively. Underlap has been incorporated in both sides in symmetric structure as well as in Drain-U and Source-U devices. The model parameters are calibrated and matched with the experimental data [18]. These devices was simulated and analyzed using 2D numerical simulator named Sentaurus TCAD from synopsys with 32 nm technology.

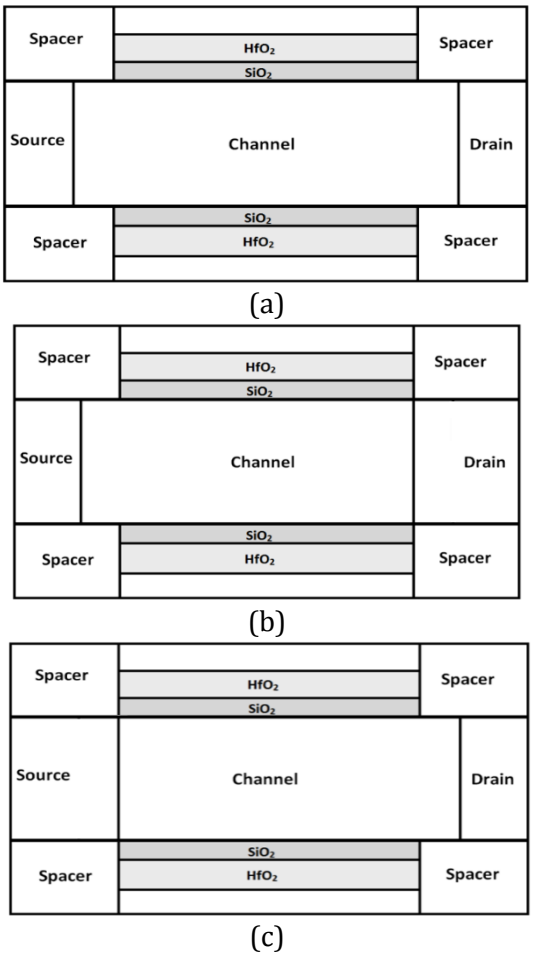

Figure 1. Cross-sectional view of different device architecture for 32 nm DG-MOSFET. (a) Symmetric-U, (b) Source-U, and (c) Drain-U.

3. ANALOG PERFORMANCE

This section presents the analog performance of three devices. The parameters like I_d, g_m, g_m/I_d, g_mR_o, and DIBL are mainly considered to evaluate the performances.

Figure 2 showcases the I_D-V_{gs} characteristics of the underlapped devices. It is evident that the asymmetric device with Drain-U exhibits the highest ON-current whereas the Symmetric-U

device shows the best subthreshold swing. This can be understood from the conduction band diagram in Figure 3. The band diagram demonstrates that while the Symmetric-U and the Source-U device shows similar barrier heights when gate voltage is applied, the Drain-U device offers no energy barrier along the channel. This results in a larger influx of electrons into the channel, and thus drastically increasing the ON-current. The Source-U device, having a lower resistive path than the Symmetric-U device, also exhibits a slightly higher ON-current. Having a higher resistive path for the symmetric device also means lower OFF-currents, which in turn results in better subthreshold swing.

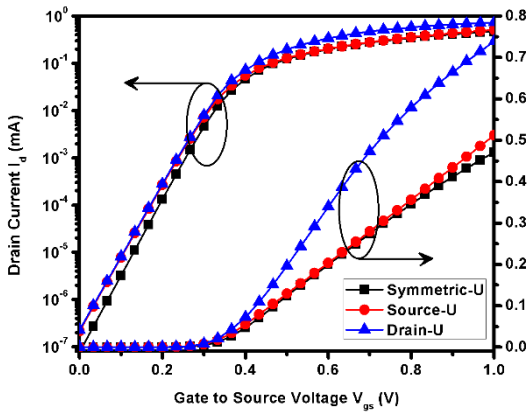

Figure 2. Transfer characteristics of different underlap configurations.

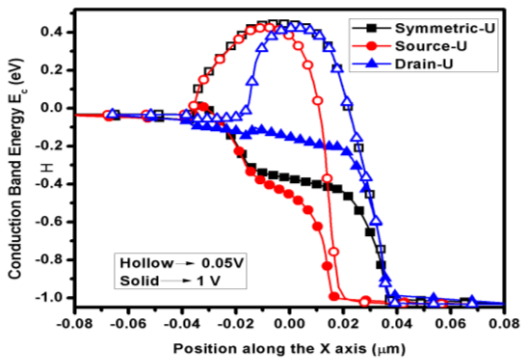

Figure 3. Representation of Conduction Band diagram for different underlap configurations at OFF state and ON state where V_{ds} = 1 V.

The g_m and g_m/I_d is presented in Figure 4. Here, again Drain-U exhibits superior g_m on account of higher ON-currents. The Symmetric-U device, however, showcases a higher g_m/I_D on account of lower subthreshold currents.

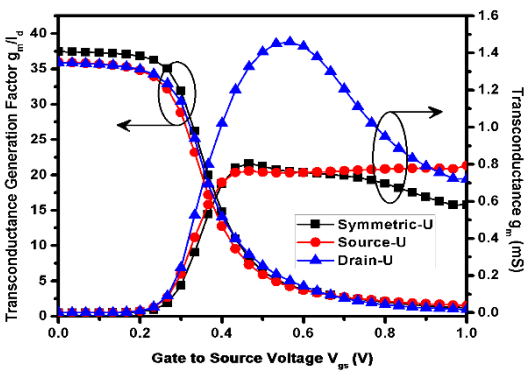

Figure 4. Variation of g_m and g_m/I_d with V_{gs} for different underlap configurations.

Figure 5 displays the g_mR_o of the MOSFETs. As discussed previously, the Symmetric-U device has a higher channel resistance on account of having underlap at both ends. Hence, the Symmetric-U-DG-GS device shows the highest g_mR_o. Among the asymmetric devices, the Source-U-DG-GS nMOSFET has the better intrinsic gain than its Drain-U counterpart.

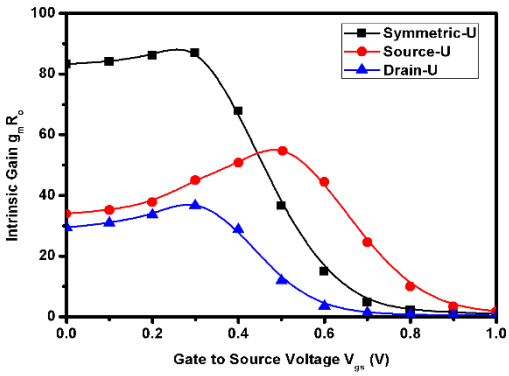

Figure 5. Variation of g_mR_o with V_{gs} for underlap configurations.

The I_D-V_{ds} characteristics of the devices are plotted in Figure 6. It is evident that the Drain-U device suffers from the highest channel length modulation due to the absence of underlap at source side to compensate for the barrier loss. Whereas, the symmetric and the Source-U devices show superior characteristics in terms of channel length modulation

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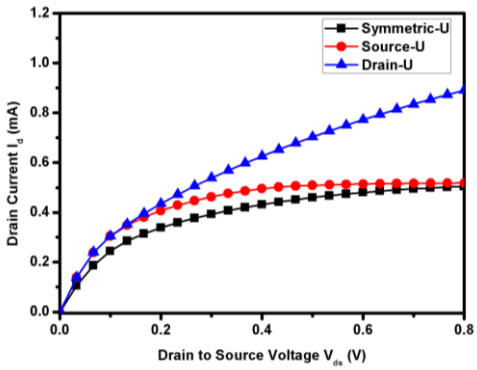

Figure 6. I_D-V_{ds} for different underlap configurations at V_{gs} = 0.55 V.

The DIBL effect on various underlap structures are shown in the bar diagram of Figure 7. This has been evaluated by calculating the change in threshold voltage upon the change in drain-to-source voltage (V_{DS}). V_{DS} considered for the evaluation are 0.05 V to 0.55 V. Figure 7 shows that while the Symmetric-U device shows the best performance, the Source-U device is the better device among the asymmetric devices.

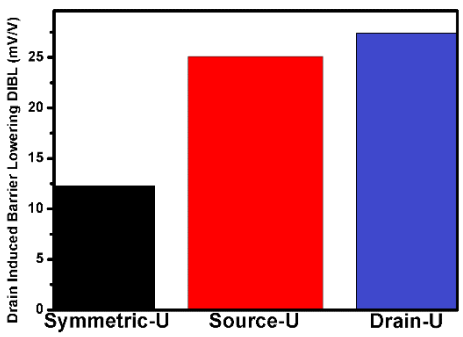

Figure 7. DIBL of three devices having different underlap configurations.

4. RF ANALYSIS

High-speed application of the proposed devices needs RF analysis. Parameters such as C_{gs}, C_{gd}, R_{gs}, R_{gd}, τ_m, f_T, and f_{max} were taken into consideration for the RF performance measurement. For the parameters extraction, the devices are kept at $V_{gs} = V_{ds} = 0.55V$ and the applied frequency is swept between 0-100 GHz. The obtained Y-parameters from the TCAD simulations are used to determine the aforementioned parameters. In order to determine the intrinsic parameters, a non-quasi static (NQS) approach was used [12]. Using the de-embedding technique [7, 12], the extrinsic components was eliminated from the Y matrix obtained from simulations. Thus, the intrinsic Y matrix (Y^{int}) was obtained from the computation done in order to get the RF parameters. The equations used to determine the RF parameters were referred from [12].

Figure 8 plots the deviation of the intrinsic capacitances against frequency. As the capacitance by nature is inversely proportional to the distance between the two electrodes, the presence or absence of the underlap region performs a vital role to determine the intrinsic capacitances of the device. Hence, C_{gd} is maximum in Source-U device where the Drain-U device is absent; whereas both Drain-U and Symmetric-U devices show lower intrinsic C_{gd}. On the contrary, the gate-to-source capacitance C_{gs} exhibits a reverse trend where Drain-U has the maximum C_{gs}.

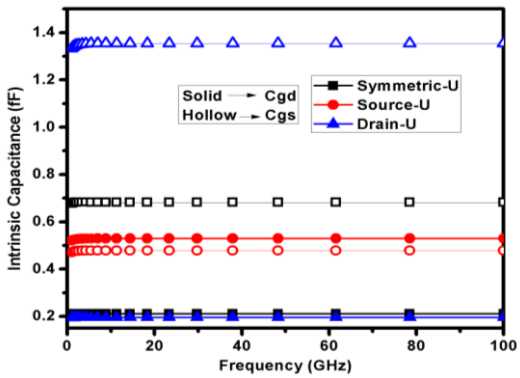

Figure 8. Depiction of C_{gs} and C_{gd} with frequency for different underlap configurations.

Figure 9 shows the variation in R_{gs} and R_{gd} with respect to frequency. The result shows the maximum amount of intrinsic resistance in the presence of underlap on both sides such as in symmetric device. Among the asymmetric devices, R_{gs} is greater for the Source-U device whereas R_{gd} is greater for the Drain-U device.

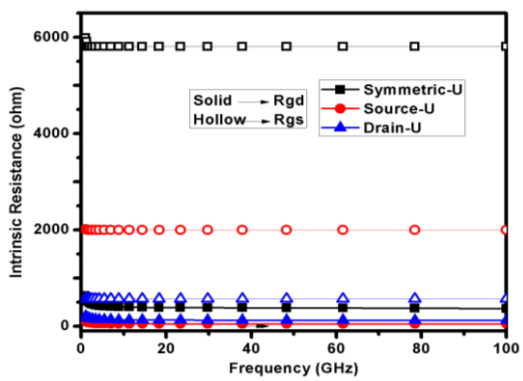

Figure 9. Representation of R_{gs} and R_{gd} with frequency for different underlap configurations.

The τ_m is presented in Figure 10. The Drain-U-DG-GS nMOSFET having the lowest τ_m outperforms the rest. This is due to the fact the electrons face no energy barrier along its path.

The Source-U has lower τ_m than the Symmetric-U device due to having the lower resistive path than the Symmetric device.

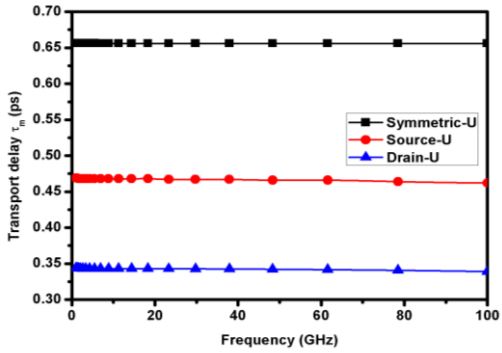

Figure 10. τ_m with frequency for various underlap configurations.

Figures 11 and 12 show the cutoff frequency f_T and the maximum frequency of oscillation f_{max} respectively. The expressions used to calculate the parameters are in [7, 12] and are as in Equation (1) and (2):

$$f_T = \frac{g_m}{2\pi c_{gs}} = f_0|H_{21}| \tag{1}$$

$$f_{max} = \frac{g_m}{2\pi c_{gs}\sqrt{4(R_s+R_i+R_g)\,(g_{ds}+g_m\frac{c_{gd}}{c_{gs}})}} = f_0\sqrt{\left(\frac{|Y_{21}-Y_{12}|^2}{4[R_e\,(Y_{11})R_e\,(Y_{22})-R_e\,(Y_{12})R_e\,(Y_{21})}\right)} \tag{2}$$

where f_0 is the operating frequency, g_{ds} R_s, R_i, and R_g are carrying their usual meaning.

Since f_T is directly proportional to the g_m, the device having the highest g_m (i.e. Drain-U) also exhibits higher cut-off frequency. The maximum frequency of oscillation also shows a similar trend.

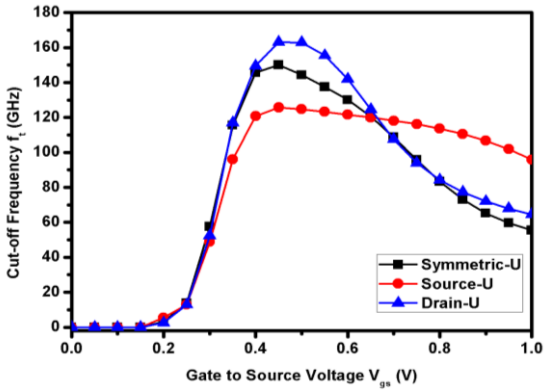

Figure 11. Variation of f_T having different underlap configurations.

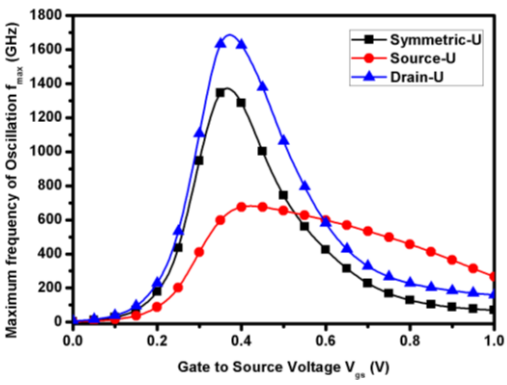

Figure 12. Variation of f_{max} for the concern devices at V_{ds} = 0.55 V.

5. CIRCUIT PERFORMANCE

Circuit performance of the three devices is presented in this section. A single stage amplifier was chosen to evaluate the performance of the proposed devices as the driver NMOS of the aforementioned circuit. A direct current (DC) sweep and small signal frequency analyses were performed on the circuit using the three devices, which are plotted in Figures 13 and 14, respectively. It is evident that the asymmetric devices exhibit a sharper transition than the symmetric device. The small signal gain is computed using the equation [18][19]:

$$\frac{V_{out}}{V_{in}} = \frac{(sC_{GD} - g_m)R_D}{R_s R_D C_{GD}\, C_{GS}\, S^2 + [R_s(1+g_m R_D)C_{GD} + R_s C_{GS} + R_D C_{GD}]s + 1} \quad (3)$$

The DC gain is the highest for the Drain-U-DG-GS nMOSFET, owing to its high g_m mainly because at lower frequencies, the parasitic capacitances have a negligible effect. Therefore, the gain has become directly proportional to the g_m of the device. As the frequency goes higher, the effect of the parasitic capacitance increases and thereafter, its effect dominate the output. Hence, the gain of the circuit falls down.

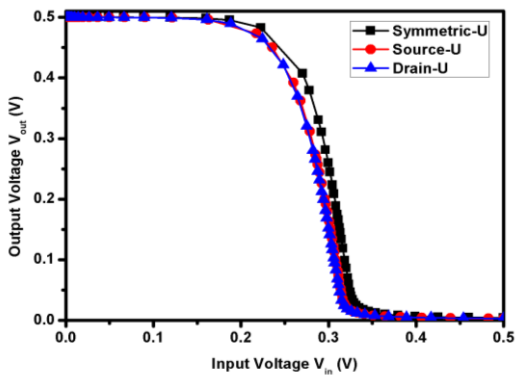

Figure 13. DC sweep analysis of single stage amplifier circuit having proposed device as driver NMOS.

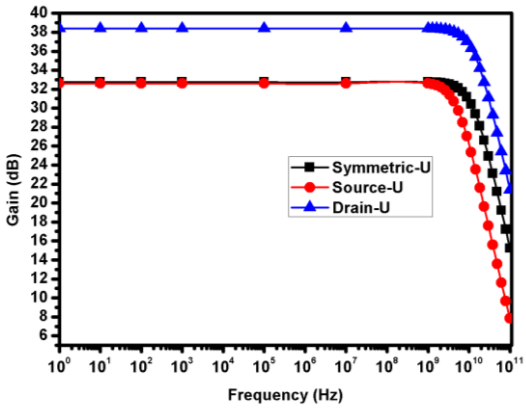

Figure 14. Depiction of gain for different underlap configurations used in a single stage amplifier.

6. CONCLUSION

This paper presents a consolidated study of different underlap architectures with respect to analog, RF, and circuit performance. Due to the lesser effective channel length, the asymmetric structures offer more ON-current and more g_m. However, it shows more SCEs than its symmetric counterpart. It is well evident that the Drain-U offers 56.86% higher I_D as well as 46.73% higher g_m making a compromise with higher DIBL and high channel width modulation. However, the Source-U showed performance improvement with respect to SCE immunity and intrinsic gain, which is fairly comparable to the device with Symmetric-U. RF analysis also shows improvement in the τ_m for the asymmetric devices. Drain-U device shows 48.32% decrease in the τ_m with respect to the symmetric device whereas, the Source-U device shows a 29.75% decrease in τ_m. Hence, the Source-U device structure shows significant improvements over the Symmetric-U device without having major suffering from severe channel length modulation and deteriorated intrinsic gain. Therefore, it is found as the most reliable device for RF applications.

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